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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAMBUS, INC.[1]
Appellant

Appeal 2010-011178
Reexamination Control No. 90/010,420
United States Patent 6,034,918
Technology Center 3900

Before SCOTT R. BOALICK, KARL D. EASTHOM, and
KEVIN F. TURNER, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL[2]

---

[1] Appellant, Rambus, Inc., is the real party in interest for this appeal.
[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" shown on the PTOL-90A cover letter attached to this decision.

Appellant, Rambus, Inc., appeals under 35 U.S.C. §§ 134(b) and 306 from a final rejection of claim 18. All other pending claims have been confirmed. (App. Br. 4.) We have jurisdiction under 35 U.S.C. §§ 134(b) and 306.

We AFFIRM.

STATEMENT OF THE CASE

This proceeding arose from a third party request for *ex parte* reexamination by Hynix Semiconductor, Inc. of U. S. Patent 6,034,918, titled "Method of Operating a Memory Having a Variable Data Output Length and a Programmable Register." Appellant's Brief lists numerous related judicial and other proceedings including *inter partes* and *ex parte* reexaminations, International Trade Commission proceedings, and Federal District Court and Circuit Court proceedings. (App. Br. 1-4.) An oral hearing of this appeal transpired on October 27, 2010 and was subsequently transcribed [hereinafter BPAI Tr.].

The '918 Patent

The '918 patent discloses a method of operating a memory device. (Abstract.)

Claim 18 follows:

18. A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:

receiving an external clock signal;

receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request;

receiving a first read request from the bus controller; and

outputting the first amount of data corresponding to the first block

size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal.

The Examiner rejected claim 18 under 35 U.S.C. 102(b) as anticipated based on the *iAPX Interconnect Architecture Reference Manual* (Intel Corp.) (1982) [hereinafter iAPX Manual].

ISSUE

The issue is whether the memory "device" recited in claim 18 reads on the memory "module" disclosed in the iAPX Manual. The central dispute turns on whether the claimed term "device" is limited to a single "chip" embodiment or also embraces a "memory stick" embodiment as disclosed in the '918 patent.

FINDINGS OF FACT (FF)

The iAPX Manual

I1. Figure 1-2 of the iAPX Manual follows:

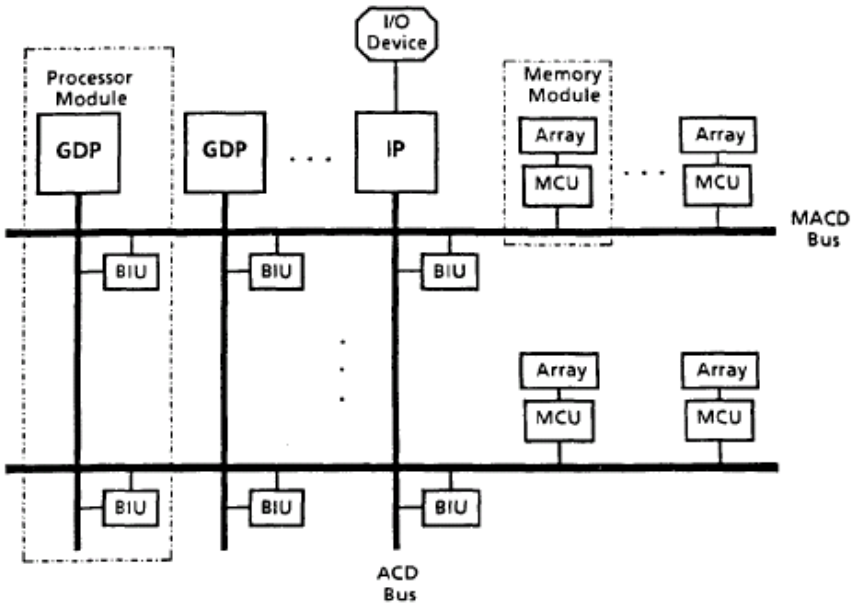

Figure 1-2. iAPX 432 Interconnect Topology F-0398

Figure 1-2 depicts a memory module comprising a memory storage array and a MCU (Memory Control Unit).

"The storage arrays will typically be constructed with high-density dynamic RAM (DRAM) components." The MCU requires a "modest amount of external logic . . . to interface the MCU to the storage array RAMs - - for simple configurations, as few as 12 external TTL packages are required." (iAPX Manual at p. 1-4.)

I2. The memory module constitutes "a memory confinement area." (iAPX Manual at p. 1-8, 3-2.)

I3. A component level constitutes the lowest level of hardware in the system, an example of which is a RAM chip. A module comprises a group of interconnected components. (iAPX Manual at p. 2-1.) The presence or absence of any module does not prevent communication between any other modules. (iAPX Manual at p. 2-6.)

The '918 Patent

D1. The '918 patent states that "[p]referred devices for use in this invention include device-type register information specifying the type of chip." (Col. 7, ll. 53-55.)

D2. The '918 patent refers to chips as devices as follows: "Fig. 8b illustrates how each device 51, 52 receives each of the two bus clock signals . . . ." (Col. 19, ll. 15-16.) Figures 8A and 8B label each device 51 and 52 as a "CHIP."

D3. The disclosed invention reduces consumed power:

> By using a single row access in a single RAM to supply all the bits for a block request (compared to a row-access in each of multiple RAMs in conventional memory systems) the power

> per bit can be made very small. Since the power dissipated by memory devices using this invention is significantly reduced, the devices potentially can be placed much closer together than with conventional designs.

(Col. 17, ll. 20-27.)

D4. Memory devices are described as subsystems: "Another unique aspect of this invention is that each memory device is a complete, independent memory subsystem with all the functionality of a prior art memory board in a conventional backplane-bus computer system." (Col. 7, ll. 19-22.)

D5. Slaves and masters are described as follows.

> [T]his invention connects master or bus controller devices, such as CPUs, Direct Memory Access devices (DMAs) or Floating Point Units (FPUs), and slaved devices, such as DRAM, SRAM or ROM memory devices. A slave device responds to control signals; a master sends control signals. Persons skilled in the art realize that some devices may behave as both master and slave at various times, depending on the mode of operation and the state of the system. For example, a memory device will typically have only slave functions, while a DMA controller, disk controller or CPU may include both slave and master functions.

(Col. 6, ll. 13-25.)

D6. A primary bus unit in the '918 patent has two or more devices, typically 32, connected to a transceiver. A primary bus unit can be mounted on a circuit board 66, sometimes called a memory stick. A primary bus unit is also a memory subsystem. The circuit board includes a transceiver device 19, two or more memory devices, and a primary bus unit 18 connecting the devices together. The circuit board connects to a transceiver bus. (Col. 19, l. 46 to col. 20, l. 15.)

"The transceivers are quite simple in function. They detect request packets on the transceiver bus and transmit them to their primary bus unit. . . . The transceivers also watch their primary bus unit, forwarding any data that occurs there to the transceiver bus." (Col. 20, ll. 16-24.)

D7. The memory subsystem allows several devices to appear as one device "by giving the system access to a contiguous block of good memory" in the several devices and using appropriate settings of address registers and pointers to the beginning and end of the block. (Col. 7, ll. 33-52.) "This is similar to prior art schemes used in memory boards in conventional back plane bus systems." (Col. 7, ll. 35-37.)

District Court Findings - Claim Interpretation for "Memory Device"

DC1. In related litigation involving the same "memory device" term in dispute here in a related Rambus patent (U.S. 6,426,916) claiming priority to the same underlying application (07/510,898) as the patent here, a District Court, modifying a previous claim construction order as to the meaning of "memory device," found, *inter alia*, as follows:

> The court remains convinced that there is no basis for reading a "single chip" limitation into the term "memory device." The specification discusses no such limit, and at various times, Rambus crafted dependent claims suggesting that a "memory device" is a broader concept than a single chip. Moreover, had Rambus meant to limit its claims to a single chip, it could have claimed a "memory chip" or used a similarly clear limitation. It chose the broad term "device," and must live with the claims it wrote.
>
> But that does not mean that the term "memory device' lacks any dimensional limit. . . . Thus, a "memory device" is limited in scale to being a component in a memory subsystem. . . . .

> This "component" interpretation of the term "memory device" is further bolstered by the detailed description. The description distinguishes "memory devices" from "processing devices." *Id*., col. 5, ll. 33-56. A "memory device" is a "complete, independent memory subsystem with all the functionality of a prior art memory board in a conventional backplane-bus system," suggesting that a "memory device" is smaller than a prior art memory board. *Id*., col. 7, ll. 23-26. . . .
>
> A person of ordinary skill in the art, reading the term "memory device" in light of the specification, would not necessarily conclude that a 'memory device' is limited to a single chip. Such a person of ordinary skill would, however, conclude that a "memory device" is constrained in its dimensions and features. A "memory device" does not include a microprocessor like a CPU or memory controller. It connects to a bus as a component in a larger system. While its size is not explicitly defined, it is on the order of a single chip, and smaller than a "memory board."
>
> . . . . [A] memory device is a component of a memory subsystem in which information can be stored and retrieved electronically. It is smaller in physical size than that of a prior art memory board and has low power dissipation so it can be closely spaced to other components of the memory subsystem such as a processing device.

Order Clarifying the Court's Construction of Memory Device 2-4, No C-05-00334 RMW (N.D. Cal. Nov. 21, 2008) (attached to App. Br. App'x as Ex. I-2) [hereinafter Claim Constr. Order].

Appellant's Expert and Testimony

M1. Appellant's expert, Mr. Murphy, describes an extensive background and qualifications in his declaration, including 35 years of experience in semiconductor devices such as, but not limited to, DRAM and SRAM design engineering and management experience. Mr. Murphy opines that skilled artisans would not refer to the iAPX memory module as a

memory device. (Murphy Decl. ¶¶ 5-10, 37-55.)[3] Mr. Murphy bases his opinion *inter alia* on the fact that the iAPX memory module contains a collection of many separate devices including a memory control unit chip. (*Id*. at ¶ 38, 45.) Mr. Murphy also concludes that a memory device "would have been readily understood by one of ordinary skill in the art to be an integrated circuit device (commonly referred to as a 'chip')" (*id*. at ¶ 46) because the '918 uses chip interchangeably with device and is concerned with accessing large blocks of data on a single chip (*id*.).

M2. Mr. Murphy also distinguishes the iAPX memory controller from an external processer and another external device, a BIU (Bus Interface Unit). The memory controller translates processor commands (from the BIU) to the DRAMs to allow data to be written to and from the DRAMs on the memory module. (*Id*. at ¶ 42.) Mr. Murphy also describes the iAPX memory controller as compensating for the functionality in the '918 patent inventive DRAMs, resulting in "a more complex memory controller" but otherwise performing functions that "enable it to deal with the conventional asynchronous DRAMs in the storage array." (*Id*. at ¶ 44.)

M3. Appellant also relies on testimony concerning the meaning of "memory device" by Mr. Rhoden introduced in an unrelated interference proceeding as described more fully below. (App. Br. 22-23; App. Br. App'x Ex. H-1 "Deposition of Desi Rhoden" (filed in App. No. 11/203,652, Mar. 12, 2007) [hereinafter Rhoden Dep.].)

[3] Reference is to Declaration of Robert J. Murphy (filed Oct. 26, 2009) as opposed to the Supplemental Declaration of Robert J. Murphy (Supp. Decl. filed Feb. 10, 2010).)

Deposition and Declaration Testimony in Other Proceedings

McA1. The Examiner (Ans. 17, n. 3) pointed to deposition testimony by Joseph McAlexander (recorded May 9, 2008 for *Rambus Inc. v. Hynix Senimconductor, Inc. et al.*, No. C05-00334 RMW (N.D. Cal.)) filed in *inter partes* Reexamination Control No. 95/001109 (listed as Exhibit O-2 in an Appendix to Rambus's Response to the '109 Office Action of August 7, 2009 (filed Nov. 9, 2009)) [hereinafter McAlexander Dep.].)

Mr. McAlexander testified that claim 18 of the '918 patent encompasses a memory module:

Q.: Is a memory module a memory device under your construction?

A.: It could be. If, again, it had - - when you look at the term "memory device" and you put it in the claim, then obviously it has to meet any limitations that are imposed by the claim, but in general, the term "memory device" does not have to be limited to a single chip, and it can apply to a module.

Q. Let's look at the '918 patent, since we marked that one.

A. Exhibit 19?

Q. Yes. And we were looking at Claim 18. And Claim 18 refers to a synchronous memory device, right?

A. Yes.

Q. Could the memory device there be a memory module?

A. It could be, as long as the method steps are met.

Q. What is a memory module, by the way?

A. The general understanding of a memory module is a common substrate upon which two or more memory chips are bonded or soldered.

(McAlexander Dep. at p. 67-68.)

McA2. A declaration by Mr. McAlexander also was filed in the just-described district court case and merged reexamination. (Listed as Exhibit O-1 in the '109 Rambus Resp. to the Off. Action) [hereinafter McAlexander Decl.].) The declaration states that Mr. McAlexander is a registered engineer with 34 years of experience in microcircuit and semiconductor design, is an inventor of 20 U.S. patents, and has experience as a design manager and engineer of memory DRAMS. (*See* McAlexander Decl. at ¶ 2 and attached curriculum vitae). Mr. McAlexander states that "[a] memory device is a device in which information can be stored and retrieved electronically," (*id*. at ¶ 66) and is not limited to a single-chip construction (*id*. at ¶¶ 66-68.) Mr. McAlexander also describes a device as "made up of stacked chips or multiple integrated circuit chips on a printed circuit board." (*Id*. at ¶ 63.)

PRINCIPLES OF LAW

The '918 patent term expired during the reexamination proceedings. Under these circumstances, rather than applying the "broadest reasonable" rule, claim construction rules as followed in infringement suits serve as appropriate guides. Conversely, "construing express claim language" "narrowly" in light of the specification contrasts with reading improper "inferential limitations" into a claim. *Ex parte Papst-Motoren*, 1 USPQ2d 1655, 1656-57 (BPAI 1986) (citation omitted). Prosecution history may shed light on claim scope for issued patents. *See Phillips v. AWH Corp.*, 415 F.3d, 1303, 1317 (Fed. Circ. 2005) (en banc) (prosecution history should be used if available); *Papst-Motoren*, 1 USPQ2d at 1657 (similar discussion)

(citation omitted); MPEP 2111.01 § I (Rev. 6, Sept. 2007) (discussing different claim interpretation rules).

In all cases, claims "must be read in view of the specification. . . . [T]he specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315. Also, "the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." (*Id.)* (internal citations omitted).

"Even when the specification describes only a single embodiment, the claims of a patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words of manifest exclusion or restriction'." *Leibel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (citation omitted).

ANALYSIS

Appellant maintains that the distinction between the inventive memory device and the iAPX memory module "rests on size and/or the number of chips." (BPAI Tr. 5.) Appellant also contends that a memory device is essentially a single chip while the Examiner contends that the '918 patent device is not so limiting. In other words, Appellant attempts to limit "memory device" to a chip or chips memory device, i.e., to a device having a fewer number of chips than the disclosed number of chips on the iAPX module. (App. Br. 15-17; BPAI Tr. 4.)

According to Appellant, the iAPX module cited by the Examiner contains at least 12 TTL packaged chips, a memory controller chip, and several DRAM chips. (App. Br. 15.) The Examiner does not contest Appellant's characterization of the approximate number of chips on the iAPX module embodiment relied upon by the Examiner. (*See* I1.) But according to the Examiner, one of the disclosed memory devices in the '918 patent includes a memory stick similarly having several chips as depicted in Figure 9. (Ans. 10, 27.) If this finding is correct, it implies that claim 18 embraces the iAPX memory module. (*See id*.) Conversely, Appellant maintains that the disclosed and claimed memory device excludes the disclosed memory stick. (App. Br. 20-21.)

Appellant also presents expert declarations and testimony to the effect that skilled artisans would have distinguished a memory device from a memory module. (*See* M1-M3.) The Examiner responds by pointing to a countervailing expert opinion rendered in a related reexamination and by explaining that Appellant's experts disagree with the district court's claim construction order (i.e., Appellant's experts maintain that a memory device requires a single chip, contrary to the district court's interpretation). (*See* Ans. 17-19 n.3; McA1.)

The Examiner also maintains that the district court's interpretation supports the Examiner. (Ans. 11; Ans. 15.) The Examiner agrees with the district court findings to the extent that a memory device is not necessarily a single chip, and further relies on the following '918 patent passage describing the memory stick embodiment depicted in Figure 9 to impart a broader meaning: "In general, each teaching of *this invention* which refers

to a *memory device can be practiced using a transceiver device and one or more memory devices*." (Ans. 10; 27-28 (emphasis added, quoting the '918 patent).)

Appellant responds that the Examiner misconstrues this sentence by ignoring the context of the full paragraph. The disputed paragraph follows (with emphasis on the disputed sentence):

> Referring to FIG. 9, each primary bus unit can be mounted on a single circuit board 66, sometimes called a memory stick. Each transceiver device 19 in turn connects to a transceiver bus 65, similar or identical in electrical and other respects to the primary bus 18 described at length above. In a preferred implementation, all masters are situated on the transceiver bus so there are no transceiver delays between masters and all memory devices are on primary bus units so that all memory accesses experience an equivalent transceiver delay, but persons skilled in the art will recognize how to implement systems which have masters on more than one bus unit and memory devices on the transceiver bus as well as on primary bus units. *In general, each teaching of this invention which refers to a memory device can be practiced using a transceiver device and one or more memory devices on an attached primary bus unit*. Other devices, generically referred to as peripheral devices, including disk controller, video controllers or I/O devices can also be attached to either the transceiver bus or a primary bus unit, as desired. Persons skilled in the art will recognize how to use a single primary bus unit or multiple primary bus units as needed with a transceiver bus in certain system designs.

('918 patent, col. 19, l. 60 to col. 20, l. 15 (emphasis added) [hereinafter D8].)

According to Appellant, "[j]ust because some features of the inventive 'memory device' can be replicated and used in a transceiver device, that

does not render the two equivalent or synonymous." (App. Br. 20.) In other words, according to Appellant, the passage clearly shows a distinction between a memory stick and a memory device. Thus, while Appellant agrees with the Examiner that "'single chip devices can be used to practice the goals of the invention'" and that "'memory boards with plural memories and other non-memory components (such as bus lines and transceivers can be used'" (App. Br. 21 (quoting Examiner's Office Action 12, Mar. 26, 2009)), Appellant asserts that "claim 18 is limited to a memory device and does not recite memory boards or other multi-chip systems that may also 'practice the goals of the invention.'" (App. Br. 21.) Appellant explains that "[o]ther claims in the Farmwald [i.e., Rambus] family, including claim 15 of U.S. Patent Nol. 6,185,644, recite a transceiver device and memory device separately." (*Id*. n.16.)

However, the passage from the '918 patent quoted *supra* indicates that such a multiple component memory board is "*sometimes* called a memory stick." (D8 (emphasis added).) Then, a couple of sentences later, the '918 patent explains that: "[i]n general, *each teaching of this invention* *which refers to a memory device*" can include "a transceiver device and *one or more memory devices*" - i.e., a memory stick. (*Id*. (emphasis added).) The next sentence creates a distinction between the disclosed memory device(s) and "*[o]ther devices*, generically referred to as peripheral devices." (*Id*. (emphasis added).) In other words, the disputed passage indicates that "this invention" includes a memory device which is *sometimes* called a memory stick and does not preclude "one or more memory devices," but a memory

device does not include "other . . . peripheral devices" such as disk controllers, video controllers, or I/O devices. (*See* D8.)

Appellant maintains that such a construction is illogical because "a set of memory devices is being equated to a 'memory device.'" (App. Br. 20). Appellant's assertion is unconvincing. The disputed passage literally equates a memory device with several memory devices. Logically, the passage equates a set of memory devices (e.g., several chips) to a memory device because the scope of the inventive memory device varies from a single chip memory device to a memory board device having multiple chips. (*See* D6). Further supporting this interpretation is the fact that the invention allows several chips to appear to the system as one (by lining up contiguous memory addresses over several chips). (D7.) Also, the '918 patent describes the disclosed memory device as typically (i.e., not always), a slave device (D5), and implies that a memory stick does not always have a master thereon (*see* D8 (the passage does not clearly indicate one way or the other if a transceiver is a master device). In any event, it is not illogical, but rather logical, to refer to such a collection of chip memory devices which act as one and which is "sometimes called a memory stick" as a memory device.

When a patent refers to "this invention" as the '918 patent does, it can imply a definition or at least set the scope for the claimed invention. *See Edwards Life Sciences LLC v. Cook Inc.*, 582 F.3d 1322, 1330 (2009) (characterizing *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys. Inc.* 242 F.3d 1337, 1343 as "construing term to include feature characterized as 'the present invention'"); *cf. Edwards*, 582 F.3d at 1330 (citing additional similar precedent and holding that the consistent interchanging of

"interluminal graft 10" with "graft 10," use of the phrase, "as defined above," and frequently describing an "interluminal graft" as "'the present invention'" or "'this invention'" created a narrowing definition of graft to mean an interluminal graft). Thus, even if the '918 patent does sometimes interchange chip and memory device as Appellant argues and the expert opines (M2), referring to another embodiment as "this invention" not only cuts against any type of *Edwards*-based limiting inference relying on such interchanging, but elicits an intent to embrace both of the embodiments described.

Bolstering this broader interpretation is the fact that the '918 patent also uses "this invention" in reference to a memory subsystem as a memory device, i.e., such as the disclosed memory stick (and by implication, the iAPX memory module), as the Examiner also found. (*See* Ans. 27-29.) "Another unique aspect of *this invention* is that *each memory device is a complete, independent memory subsystem* with all the functionality of a prior art memory board in a conventional backplane-bus computer system." (D4 (emphasis added).) Appellant explains that this sentence contrasts prior art memory boards because the invention puts the function of such a board into a compact memory device: "Indeed, it would not have been necessary to note that a memory device is unique in that it has the 'functionality' of a memory board if in fact it could be a memory board." (App Br. 19; *see* Ans. 27-29 (responding).) This argument is unconvincing because it ignores the memory stick embodiment, a subsystem.

The '918 patent distinguishes its inventive memory stick from a prior art memory board. Appellant's argument implies it must do so in terms of

function, because it cannot do so in terms of any disclosed "compactness." In other words, any implied argument that the disclosed invention precludes all prior art memory boards but includes the disclosed memory (stick) board lacks a clear demarcation in terms of size or chip numbers (i.e., as opposed to a distinction based on disclosed function), and thereby eviscerates any distinction over the iAPX memory module.[4] Further, the record indicates that one disclosed uniqueness in function resides in how the memory stick transceiver interacts and accesses the memory chips on the memory board. (*Compare* M2 (Appellant's expert contrasting more complex controllers) *with* D6 (describing the simple function of transceivers).)

In a similar vein, the Examiner found that the central features which render the '918 patent's disclosed memory devices distinct over prior art chips or memory boards, i.e., the response by the chip or memory stick to an external clock, are performed by iAPX memory module. Appellant does not challenge this finding. Such a finding implies that the iAPX module is distinct from typical prior art memory boards and also implies that claim 18 reads on the iAPX module. (*See* Ans. 28.)

In further response to the Examiner's reliance on the '918 patent's definition of a memory device as "a complete, independent memory subsystem" (D4), Appellant argues that "[n]ot all memory subsystems are memory devices, and claim 18 is directed to a "memory device," not a "memory subsystem." (Reply Br. 11.) Appellant explains that "as the

[4] Apparently, based on the arguments and findings presented, it appears that the Examiner and Appellant consider the iAPX memory module to constitute a separate board, though it appears it may alternatively simply be confined to a specified board area (*see* I2).

district court recognized, the specification and claims establish that a 'memory device' is a component of a memory subsystem." (*Id*. n. 8.) Appellant also argues that the "Examiner's allegation that the specification equates 'memory device' with 'memory subsystem' is contrary to the evidence." (Reply Br. 12.)

Notwithstanding the district court's finding and Appellant's arguments, the '918 patent *specifically states* that "*each memory device is a complete, independent memory subsystem*." (D4 (emphasis supplied).) Appellant's arguments contradict descriptions in the '918 patent. Each memory device in the '918 patent is described as a complete subsystem. The '918 memory stick and chip embodiments, like the iAPX memory module, each constitute a complete subsystem with a defined area – and each one facilitates communication to memory. (*See* D5-D7, I2, I3.)

On the other hand, Appellant also argues that "the fact that the specification notes that the *inventive* memory device is a memory subsystem does not mean that all memory subsystems are memory devices." (Reply Br. 11 (emphasis added).) Appellant's arguments, viewed together, contradict each other. That is, Appellant argues here that the "inventive memory device," presumably the chip embodiment, constitutes a memory subsystem, but this argument contradicts Appellant's argument *supra* that the memory chip device is not a memory subsystem. Adding to the confusion is the use of the word "inventive," which implies that Appellant refers to both inventive embodiments; i.e., the disclosed stick and chip embodiments.

At the least, based on the foregoing discussion, Rambus did not clearly limit a memory device to a single chip memory device as described

in the '918 patent. Under analogous circumstances involving the '918 patent, our reviewing court held that the ordinary term "bus" could not be read restrictively as a "multiplexed bus" even though the patentee described the "present invention" in terms of a "multiplexed bus" in isolated portions of the specification because "the remainder of the specification and the prosecution history shows that Rambus did not *clearly* disclaim or disavow such claim scope in this case." *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094-95 (Fed. Cir. 2003); *accord Leibel-Flarsheim*, 358 F.3d at 906 ("[T]he claims of the patent will not be read restrictively unless the patentee has demonstrated a *clear intention* to limit the claim scope using 'words of manifest exclusion or restriction'." (Emphasis added)).

Appellant also argues that the Examiner's claim construction, "device(s) that allows for the electronic storage and retrieval of information," is one that the district court narrowed and is broader than any proposed by Hynix. (Reply Br. 7, n. 6.) To the contrary, according to Appellant, Hynix proposed "one or more integrated circuit components, operating as a unit, in which electronic information can be stored and retrieved from one or more arrays." (*Id*. at n. 6.) The Hynix definition coincides with the Examiner's. Both read on the chip and memory stick embodiments, as well as the iAPX memory module. (*See* Ans. 22-23 (finding that Hynix proposed a definition embracing a "multi-chip memory such as a memory board").) The district court definition also reads on the chip and stick embodiments, but does not read on all prior art memory boards (whatever they encompass).

However, Appellant does not argue that a distinction exists between the '918 patent disclosed memory stick and the iAPX controller. The disclosed memory stick comprises from two to thirty-two devices (D5), with the latter number similar in number to the iAPX memory module according to Appellant's arguments mentioned *supra*. Hence any size distinction or chip number demarcation between a stick and a module lacks a clearly supported demarcation.[5]

[5] The district court found that "a 'memory device' does not include a microprocessor like a CPU or memory controller. It connects to a bus as a component in a larger system." (DC.) The district court also found that a memory device is constrained in its features and dimensions and is "smaller in physical size than that of a prior art memory board." (DC.) These findings do not preclude the '918 patent memory stick from being a memory device because the stick connects as a component to a larger bus and apparently, the transceiver is not necessarily a processor. That is, the transceiver performs simple control functions such as passing data. (D6.) According to Appellant, even the chip memory devices include an integrated multiplexor, a driver, and other circuitry to control data. (Reply Br. 12.) And as noted *supra*, Appellant makes no distinction about the extent of the memory control functions, and argues based only on size and/or chip number (BPAI Tr. 5). Appellant also states that the disclosed and claimed integrated chip does not preclude and requires certain control circuitry within it. (BPAI Tr. 3.) The iAPX memory control unit (MCU) (I1) within the MCU performs similar functions, even if more complex, than that of the transceiver or internal logic of the chip; i.e., the iAPX controller receives and translates instructions from an external processor, the BIU, according to Appellant's expert, Mr. Murphy. (*See* M2 and the "*Expert Testimony*" discussion *infra.*) Hence, it is not clear if the district court's definition of memory device would preclude the iAPX memory module based on its internal memory controller, where the iAPX external BIU performs more like a microprocessor mentioned by the district court as precluded.

Expert Testimony

Appellant's Brief does not point to expert findings specifically responding to the Examiner's findings relying on the '918 patent Figure 9 memory stick subsystem embodiment as embraced by claim 18. (*See* M1; App. Br. 19-21.) According to Appellant's expert Mr. Murphy, the iAPX controller memory module is distinct from a BIU (bus interface unit) or processor, transfers data to and from the DRAMs from the BIU processor, and performs complex functions, but performs data transfer functions similar to the '918 patent's memory devices. (M1; *accord* App. Br. 12-13; note 5 *supra*.) In other words, the '918 patent's chip and transceiver embodiment each function similarly to the iAPX memory controller of the memory module, with perhaps varying degrees of complexity. As such, Mr. Murphy's opinion does not contradict the Examiner's finding regarding the Figure 9 embodiment disclosed in the '918 patent.

Appellant also relies on testimony by Mr. Rhoden in an unrelated interference proceeding concerning the scope of the term "memory device," apparently as it relates to a "Drehmel" device or patent. (*See* M3.) Mr. Rhoden testified under cross-examination that "[w]ith respect to Drehmel, I think memory and memory device would perhaps be the same thing," that "in the context here" there is "probably . . . very little difference" "between memory device and memory chip." (Rhoden Dep. 45.) Mr. Rhoden also testified that "a card that has multiple package memory chips" is typically not a "memory device" or a "memory system." (*Id*. at 46.) Mr. Rhoden also testified that "[t]ypically, a memory module would be a credit circuit board or something like that that would have, among other things, perhaps memory

devices on it." (*Id*. at 109.) Mr. Rhoden also testified that "a [memory] 'module' has a wide variety of meanings," (*id*. at 110) and that "in certain instances" a "memory module" and "a memory subsystem" could be the same (*id*. at 110.)

The Examiner found that the context of this testimony surrounding another ("Drehmel") patent or device is not clear, whereas Appellant countered that the context is not important because the testimony simply shows a difference between a memory module and a memory device, and establishes a plain meaning for the term "memory device" because "typically" means "customary and ordinary." (Reply Br. 13, n. 10.) The context here, however, is critical because the testimony does not address the Examiner's finding regarding the scope of the term in the '918 patent, and in particular, the scope in light of the Figure 9 memory stick embodiment, or the fact that all memory devices in the '918 patent, including chips and sticks, are described as complete subsystems. (*See* App. Br. 22-23.) And the testimony indicates that "in the context here," i.e., "with respect to Drehmel," there is "probably very little difference" between a device and a chip. (Rhoden Dep. 45.)

Moreover, as just noted, Mr. Rhoden states that a memory module may constitute a memory subsystem and has a wide variety of meanings and further states that a device is not typically considered to be a card, thus implying that a device can be considered to be a card or a module (i.e., under the right circumstances). Because the '918 patent memory devices include memory subsystems, it follows that memory modules - subsystems

according to Mr. Rhoden's testimony - are embraced by the term "memory devices."

The Examiner also countered with testimony by Mr. McAlexander to show that a memory device can be a memory module. Mr. McAlexander opined that claim 18 of the '918 patent encompasses a memory module. (Ans. 17, n. 3; McA1.) Appellant describes this testimony as not credible, *inter alia*, because Mr. McAlexander disagreed with our reviewing court's finding (i.e., in *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d at 1090-91) that an integrated circuit device is properly construed as a chip. (Reply Br. 14, n. 11.)[6] However, under Appellant's standard, Mr. Rhoden's

[6] Appellant also points out that the Examiner listed this deposition testimony for the first time in the Answer and it is not of record in this proceeding. However, Appellant does not object to it, *id.*, and further, Appellant listed the underlying district court proceeding (No. 05-00334 RMW (N.D. Cal.)) and the merged reexamination proceeding (95/001,109 and 95/001,155) involving this deposition in the Brief, describing those proceedings as related to the instant proceeding. (App. Br. 1, 4.) Appellant's Reply Brief also asserts that Hynix employed Mr. McAlexander as an expert in several related reexamination proceedings, but "[Mr. McAlexander] has not offered an opinion on the construction of the term 'memory device' in those declarations." (Reply Br. 14 n. 11). To the contrary, Mr. McAlexander's declaration does include a definition (or two) for a "memory device." This declaration appears in the same litigation and reexamination and was attached to the same Rambus response as the deposition. (*See* McA2.) By raising an asserted lack of a proffered definition in the Reply Brief after submitting the declaration showing otherwise in a related proceeding, even though the Examiner does not rely on the declaration, Rambus cannot complain of its use or claim surprise, whether used only to contradict the assertion made, or as substantive evidence. In any event, it is considered to be cumulative to (or shed light on in view of the assertion) the deposition testimony (McA1), and is not required to support our ultimate decision. When queried about Mr.

testimony also would not be credible because it contradicts the district court finding that a memory device is not necessarily limited to a single chip.

Prosecution History Including Related Proceedings

Appellant and the Examiner refer to several related proceedings to support their respective positions. For example, Appellant notes that the Examiner, in a related proceeding (Reexam. Cont. No. 90/010082 involving the Rambus 6,038,195 patent), found as follows: "The Examiner notes that the patent specification makes it clear that the memory devices refer to the memory chip itself." (App. Br. 18.) The Examiner responds by stating that the finding was later clarified in that the Examiner was only referring to specific chip embodiments. (Ans. 28-29.) The '082 record also shows that the '195 patent claims were allowed for other reasons.[7] Appellant's Reply Brief does not address the Examiner's clarification.

McAlexander at the BPAI oral hearing, Appellant's counsel there candidly described him as simply a hired expert (as compared to the "neutral" Mr. Rhoden) and that he (counsel) had "no other explanation other than he [Mr. McAlexander] has a different opinion." (BPAI Tr. 12.)

[7] The Examiner's (partial) clarification follows:

> As noted previously, the Examiner maintains that the patent specification does not define the broad term 'memory device'. However, the Examiner acknowledges that the memory devices such as ROM, SRAM and DRAM are defined as being a single integrated memory chip. No definition or statement has been shown with respect to the much broader 'memory device' term.

(Reexam. Control No. 90/010,082, Office Action 21 (RXNIRC) (Feb. 5, 2010).) *See id*. at 11-15 for reasons for confirmation.

Appellant also argues that the prosecution history of the U.S. 5,954,804 patent shows a clear demarcation between memory module and device, thereby rendering the Examiner's construction meaningless. (App. Br. 30-32.) During prosecution of the U.S. 5,954,804 patent, Rambus argued that "[i]n contrast to the present invention, memory devices of the prior art did not include an internal register for storing a [sic] identification value." (App. Br. App'x Ex. D-1 (App. No. 08/798,525, Supp. Prel. Amend. 12 (filed Feb. 3, 1999).) Rambus also argued that "the Weymouth patent is applicable to assigning unique identification values to a memory module or card (i.e., the peripheral device) and not applicable to (and incapable of) assigning a unique identification value to an individual memory device on the module or card." *Id*. at 14.

These arguments show only that Rambus facially, at most, made the distinction argued, because the arguments were in the context of the inventive memory device having an *internal* register. (*Accord* App. Br. 30-31 (discussing the prosecution arguments).) This distinction is critical because an internal register is recited in each independent claim in the '804 patent and the term "internal register" may imply a chip device with a register internal thereto, especially in light of the '804 patent. It is also unclear how Weymouth's system identifies peripheral cards. For example, it is entirely plausible that Weymouth's system assigns an identification address or number to a port or some device *external* to each of the peripheral cards (and then identifies the attached peripheral device by its mere attachment to the port).

As the Examiner reasoned, Rambus describes Weymouth as lacking in any detail as to the interface cards and Weymouth "was not directed to any memory device at all as acknowledged by the Patent Owner." (Ans. 39.) In other words, Rambus did not contrast Weymouth's memory card or module from Rambus's claimed memory device reciting an *internal* identification register, because Rambus did not concede that Weymouth's module or board discloses or suggests a similar *internal* identification register on that module or board. As such, Rambus did not contrast (in a substantive manner having bearing here) a memory module from a memory device.

Our reviewing court specifically cautioned against reading too much into isolated remarks that Rambus made during prosecution of the '804 patent. *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d at 1090-91 (stating that "a reasonable competitor would not rely on an untrue statement in the prosecution history over the express terms in the claims," that claims control over "a loose remark in the course of prosecution," and defining the claim term "integrated circuit device" as a "circuit constructed on a single monolithic substrate, commonly called a 'chip'" (citations omitted)).[8] As the Examiner noted, the '804 patent recites claims directed to "a memory device or an integrated circuit having memory." (Fin. Rej. 13 (Dec. 11, 2009).) As the Examiner also reasoned, this implies a distinction between the broader memory device and an integrated circuit chip. (*See id*.)

The Examiner apparently concedes that in the underlying prosecution of the '918 patent, Appellant facially distinguished a memory device from a

[8] By "untrue," in context, the court seems merely to have meant an "incorrect description." *Id*.

memory board, but any distinction applies only under the specific circumstances argued. (*See* Ans. 37.) As the Examiner also correctly notes, Rambus presented other arguments distinguishing the claims and the record does not show that the USPTO relied on a distinction solely between a memory module and a memory device. (*See* Ans. 34-36.)

Moreover, the Examiner identified a critical argument Rambus made during prosecution of the '918 patent which equates a memory device with a memory module. (Ans. 37.) That is, Rambus argued that the "*memory devices or memory modules* employed in [a prior art patent to] Jackson *do not receive the clock signal* (CLK A) nor do they provide the data synchronously with respect to that clock signal." (Ans. 36 (quoting App. Br. App'x Ex. M-3, Serial No. 09/252997, Amend. 11, Jul. 23, 1999) (emphasis added).) In response, Appellant characterizes the Examiner's finding as taking Rambus's argument out of context. (Reply Br. 16-17.)

That is, Appellant explains that Rambus distinguished Jackson during the '918 prosecution based on the notion that Jackson's BIU, a separate device from the memory device, performed the functions necessary to meet the claim. (Reply Br. 17.) But as the Examiner points out, the iAPX system at issue here, like the system in Jackson, also employs a BIU which is external to the iAPX memory module, and the Examiner here is not relying on the separate BIU as part of the claimed memory device - contrary to what the examiner relied upon (i.e., the separate Jackson BIU) during the underlying '918 patent prosecution. (Ans. 35 ("As acknowledged by the Patent Owner, a device outside of the memory module was relied upon [during the underlying patent prosecution] (i.e., the BIU). The Examiner

agrees that a BIU is not part of a memory module and . . . it does not meet the Examiner's interpretation of memory device.").)

Hence, in the context of a separate BIU advanced by the previous examiner as meeting claim 18 during the underlying prosecution, Rambus's prosecution history arguments tending to equate a memory module and device make sense (and parallel Rambus's arguments over Weymouth discussed *supra*). A BIU which is separate from a memory array (i.e., not on the same card, board, or within the same module) does not constitute a part of a memory module or a memory device. Appellant's assertion that Jackson's separate BIU performs the required claim functions argued (Reply Br. 17) only bolsters the Examiner's rationale that a complete memory module which has within it an on-board memory controller (as opposed to an external or off-board BIU) and performs controller functions within the module as a unit constitutes a memory device. In other words, unlike the BIU and array in Jackson, but like the memory device in the '918 patent, the iAPX memory module is confined to its own area, receives commands from an external processor (i.e., the BIU (M2)), and also does not impact communication to the other devices of the system if removed. (I2, I3.)

Appellant's arguments show that Rambus did not make clear distinctions in the '918 patent prosecution. That is, despite any arguments superficially making a distinction, the argument *supra* states clearly that memory devices or modules in Jackson do not receive a CLK signal. So despite whatever other arguments were made, the noted argument implicitly equates a device with a module.

Other Claims in Rambus Patents

Appellant and the Examiner each point to claims in related patents to support their respective positions. For example, as mentioned *supra*, Appellant relies on claim 15 of the Rambus (i.e., Farmwald) '644 patent to show that a transceiver device and memory device are distinct because each is recited separately in the claim. (App. Br. 21 n.16; *see* Ans. 39-40 (responding to Appellant and discussing other Rambus claims).) To the contrary, such a claim and other claims by Rambus in related patents only show that when a combination claim recites both a memory device and another specific device (e.g., a transceiver), that claim indicates that a memory device is distinct from such other recited device *as regards that claim*. But when, as here, claim 18 recites a memory device without another disclosed device, the claim implies that all disclosed memory device embodiments are encompassed by the broad recited term "memory device." One such disclosed embodiment is a memory stick.[9] As the Examiner further noted, Appellant directed at least one claim more narrowly to a "memory (DRAM) device" in claim 3 of U.S. 5,841,715, thereby implying a memory device is broader than a chip. (Ans. 40.)

Summary and Concluding Remarks

Appellant's experts do not address, much less rebut, the Examiner's finding that a memory device includes a memory stick and that the '918 patent describes each as a memory subsystem. The sum total of the expert

[9] Method claim 18 here also recites a memory device "receiving . . . information from a bus controller." This bus controller limitation is not argued by Appellant as lacking from the iAPX Manual. In any event, the Examiner found that the BIU or some other external controller in the iAPX Manual corresponds to the bus controller of claim 18. (*See* Fin. Rej. 12.)

opinions unremarkably reveals that the meaning of "memory device" depends on the context. The prosecution history also does not favor Rambus; Rambus equated a memory module with a memory device. The intrinsic evidence with respect to the '918 patent indicates that a memory device is a subsystem and includes a memory stick subsystem.

As the district court found, claim 18 does not recite a chip device and the patentee must live with the broader memory device term recited. (DC1.) While our claim interpretation may not completely coincide with the district court's interpretation, the court also emphasized "the wisdom of an iterative approach to claim construction." (Claim Constr. Order at 2 (citing *Finisar Corp. v. DirecTV Group, Inc*. 523 F.3d 1323, 1329 (Fed. Cir 2008).) And while it appears that the district court claim interpretation may focus on the chip embodiments or slight variants therefrom for the term "memory device," the interpretation does not necessarily preclude the memory stick embodiment that the Examiner advanced here. For example, the district court's definition would allow for a handful of memory chips, and presumably a transceiver (because the transceiver does not appear to be a "microprocessor" or a CPU (*see supra* note 5)), but how many chips the district court's definition encompasses is unspecified, i.e., it is defined to be on the order of a chip, but not just a single chip. (*See* DC1.) Conversely, skilled artisans would have recognized that the iAPX memory module can be practiced with less than 32 chips (even assuming arguendo that Appellant correctly characterizes 32 as number of chips in the disclosed iAPX embodiment). And the module's memory control unit, the MCU, also does not appear to be a "microprocessor" or CPU (by inference based on a

description by Appellant's expert, Mr. Murphy, explaining that the MCU receives and merely translates instructions from the external BIU processor (*see* M2; note 5 *supra*)).

In any event, notwithstanding the district court findings, Appellant here makes no distinction based on transceiver or MCU functions, with the distinction argued here based only on size and/or the number of chips. If a memory device covers from one to a handful of chips as the district court found, the lines of demarcation between a memory device, a memory stick, and a memory module, in the context argued here involving memory subsystems, range from unclear to nonexistent. And Appellant bears the burden of establishing a clear demarcation as *Infineon* implies and *Morris* makes clear; i.e., "[i]t is the applicants' burden to precisely define the invention, not the PTO's," *In re Morris*, 127 F.3d 1048, 1056 (Fed. Cir. 1997). To Appellant's credit here, perhaps recognizing this blurring of the lines, Appellant attempts to limit the claim precisely to a single chip by argument, but the evidence does not support that argument.

As discussed *supra*, in the '804 patent, Rambus drafted claims to two distinct sets of claims covering 1) a memory device and 2) an integrated circuit having memory (i.e., reciting "[a] synchronous memory device" in independent claim 1, and "[a]n integrated circuit device" in independent claim 15). *Infineon*, 318 F.3d at 1091 held that an integrated circuit means a chip in the '804 patent. To hold here that a device also means a single chip as Appellant urges would mean that the terms "device" and "integrated circuit" mean the same thing in light of the '918 patent. Appellant here did not establish that the term "memory device" has a similar standard level of

an industry accepted plain meaning as *Infineon, id.* (citing two trade dictionaries) found to be the case for an integrated circuit, and did not establish a clear limiting definition in the '918 patent. The two distinct sets of claims in the '804 patent plainly indicate that Rambus considers a memory device and chip to be distinct (as the district court found).

CONCLUSION

Based on the intrinsic and extrinsic evidence of record, in light of the '918 patent, the memory device recited in claim 18 reads on the iAPX memory module.

DECISION

The Examiner's decision to reject appealed claim 18 is affirmed.

AFFIRMED

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